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REDUCING LATENCY WHEN ACCESSING TASK PRIORITY LEVELS

ABSTRACT OF THE DISCLOSURE

One embodiment disclosed relates to a method of reducing access latency to a task priority register (TPR) of a local programmable interrupt controller unit within a microprocessor. A command is received to write an interrupt mask value to the TPR, and the interrupt mask value is written to the TPR. In addition, the interrupt mask value is also written into a shadow copy of the TPR. The shadow copy is written each time that the TPR is written. Another embodiment disclosed relates to a method of reducing a latency to read a TPR of an IPF type microprocessor. When a command is received to read an interrupt mask value from the TPR, the interrupt mask value is read from the shadow copy at a memory location, instead of from the task priority register itself.